

# CMOS: Working, Construction and Applications

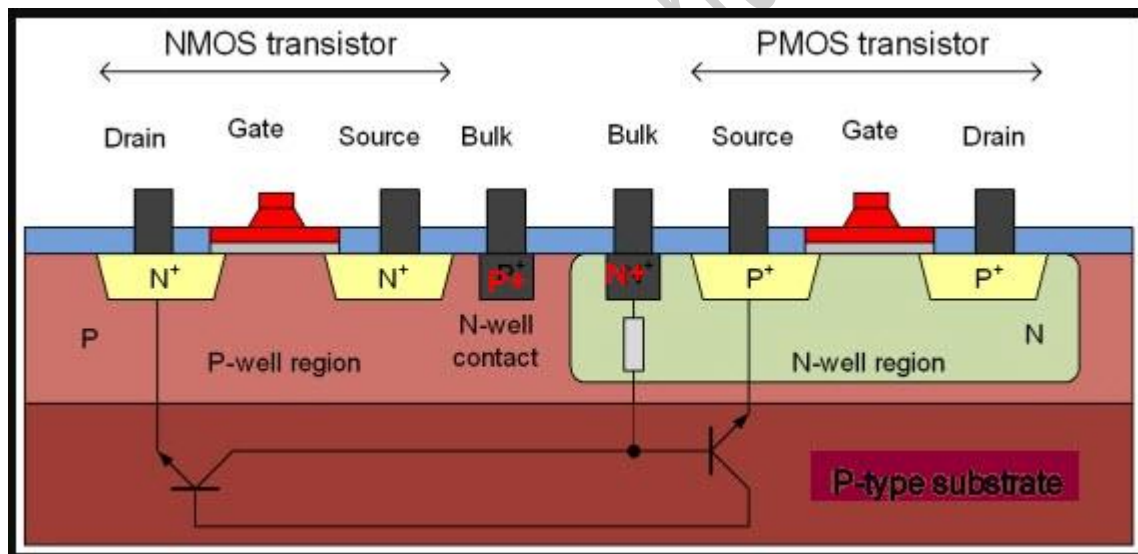
## CMOS Working Principle and Applications

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today’s computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices.

One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

## CMOS (Complementary Metal Oxide Semiconductor)

The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistor consists of P-channel MOS (PMOS) and N-channel MOS (NMOS). Please refer the link to know more about the fabrication process of CMOS transistor.

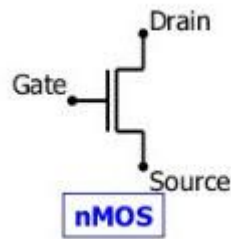


## NMOS

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS are considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

# CMOS: Working, Construction and Applications

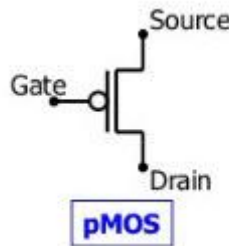
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**NMOS Transistor**

## PMOS

P- channel MOSFET consists P-type Source and Drain diffused on an N-type substrate. Majority carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.



**PMOS Transistor**

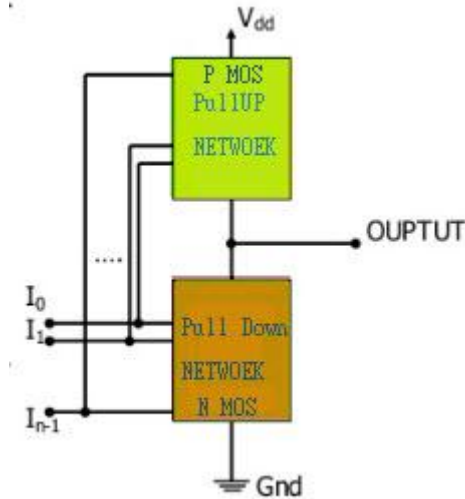
## CMOS Working Principle

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail ( $V_{ss}$  or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named  $V_{dd}$ ).

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.

# CMOS: Working, Construction and Applications

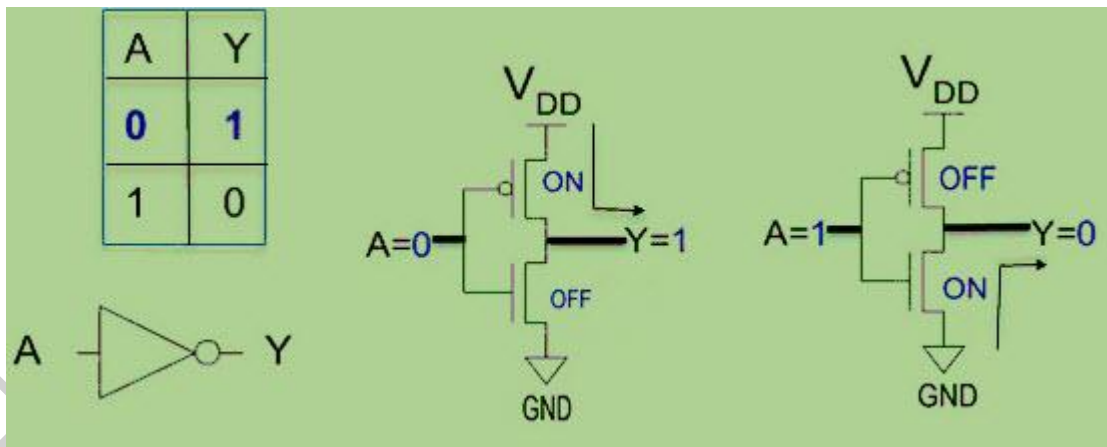


**CMOS Logic Gate using Pull-Up and Pull-Down Networks**

CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed). Furthermore, for the better understanding of the Complementary Metal Oxide Semiconductor working principle, we need to discuss in brief about CMOS logic gates as explained below.

## CMOS Inverter

The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.



**CMOS Inverter**

The NMOS transistor has an input from  $V_{SS}$  (ground) and PMOS transistor has an input from  $V_{DD}$ . The terminal Y is output. When a high voltage ( $\sim V_{DD}$ ) is given at input terminal (A) of the inverter, the PMOS becomes open circuit and NMOS switched OFF so the output will be pulled down to  $V_{SS}$ .

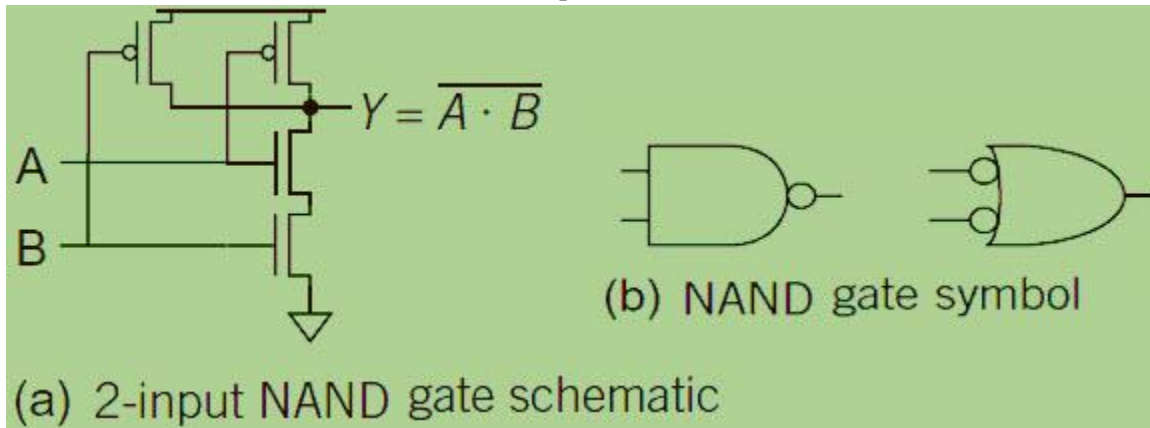
When a low-level voltage ( $<V_{DD}$ ,  $\sim 0V$ ) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes  $V_{DD}$  or the circuit is pulled up to  $V_{DD}$ .

## CMOS: Working, Construction and Applications

INPUT	LOGIC INPUT	OUTPUT	LOGIC OUTPUT
0 v	0	Vdd	1
Vdd	1	0 v	0

### CMOS NAND Gate

The below figure shows a 2-input Complementary MOS NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.



**CMOS NAND Gate**

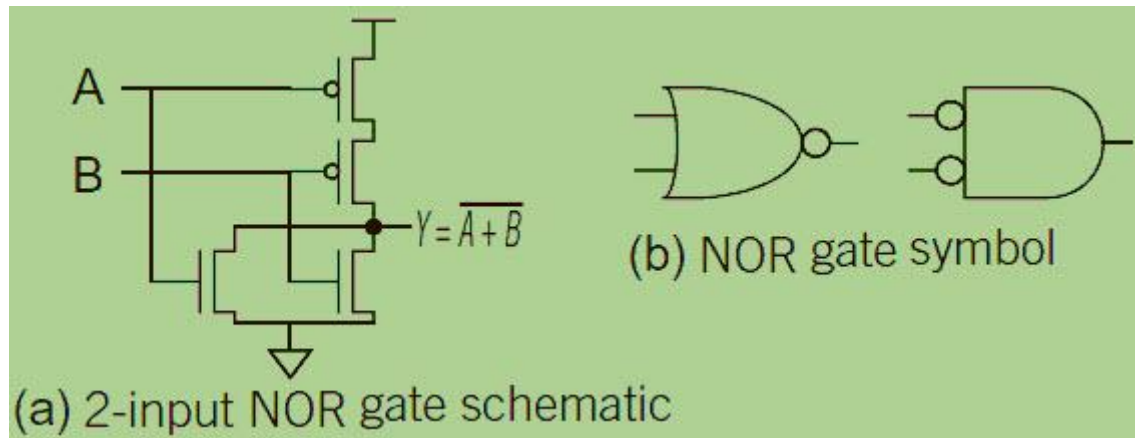
If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.

Hence, the output Y will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low. The truth table of NAND logic gate is given in below table.

A	B	Pull-Down Network	Pull-up Network	OUTPUT Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

### CMOS NOR Gate

A 2-input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in below table. The output is never left floating.



Complementary MOS NOR Gate

The truth table of NOR logic gate given in below table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

### CMOS Applications

Complementary MOS processes were widely implemented and have fundamentally replaced NMOS and bipolar processes for nearly all digital logic applications. The CMOS technology has been used for the following digital IC designs.

- Computer memories, CPUs
- Microprocessor designs
- Flash memory chip designing
- Used to design application-specific integrated circuits (ASICs)

# MOSFET: Depletion Type

## DEPLETION-TYPE MOSFET

There are two types of FETs: JFETs and MOSFETs. MOSFET is **Metal Oxide Semiconductor Field Effect Transistor**

MOSFETs are of two types based on their construction and operations, namely

- Depletion type
- Enhancement type.

## N Channel Depletion type MOSFET

### Basic Construction

A p type of semiconductor material (Si) is used as a substrate. Usually, the substrate is internally connected to the source terminal.

The drain and source terminals are connected to the n type regions through the metallic contacts.

The n type regions are linked with each other by an n channel. The gate terminal is insulated from n channel by a thin  $\text{SiO}_2$  layer.

### Effect of Insulating $\text{SiO}_2$ layer

Due to  $\text{SiO}_2$  layer between Gate terminal and n type channel, the input impedance of MOSFET is very high. Due to high input impedance, the gate current  $I_G=0$ .

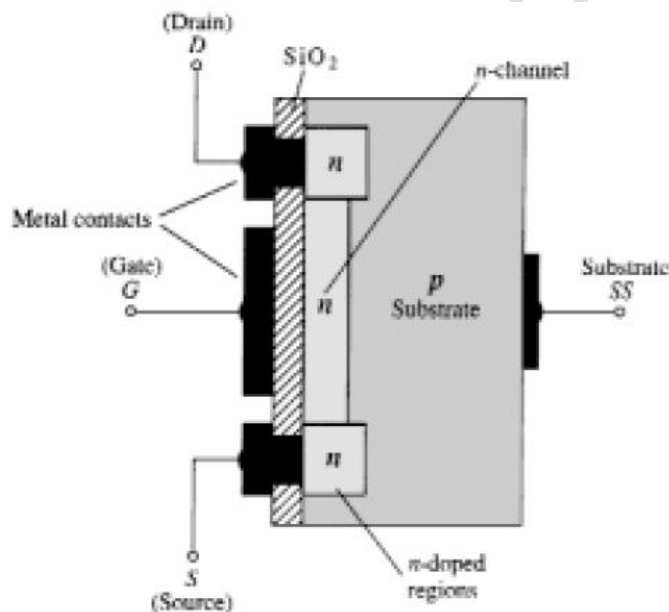


Fig 1

## Operation of n channel Depletion MOSFET

### 1. Operation with $V_{GS}=0V$

Fig 2 below shows that GATE, SOURCE and SUBSTRATE terminals are connected together at the ground potential. Thus,  $V_{GS} = 0V$ .

A positive voltage  $V_{DS}$  is applied between drain and source. Due to the positive voltage, free electrons from the channel are attracted to the drain and drain current  $I_D$  starts flowing as shown in Fig 2. As we keep on increasing the  $V_{DS}$ , the drain current increases linearly with the  $V_{DS}$ , but after a certain voltage called as **Pinch Off Voltage  $V_p$** , the drain current becomes constant. The voltage after which the drain current becomes constant is called as Pinch off Voltage.

## MOSFET: Depletion Type

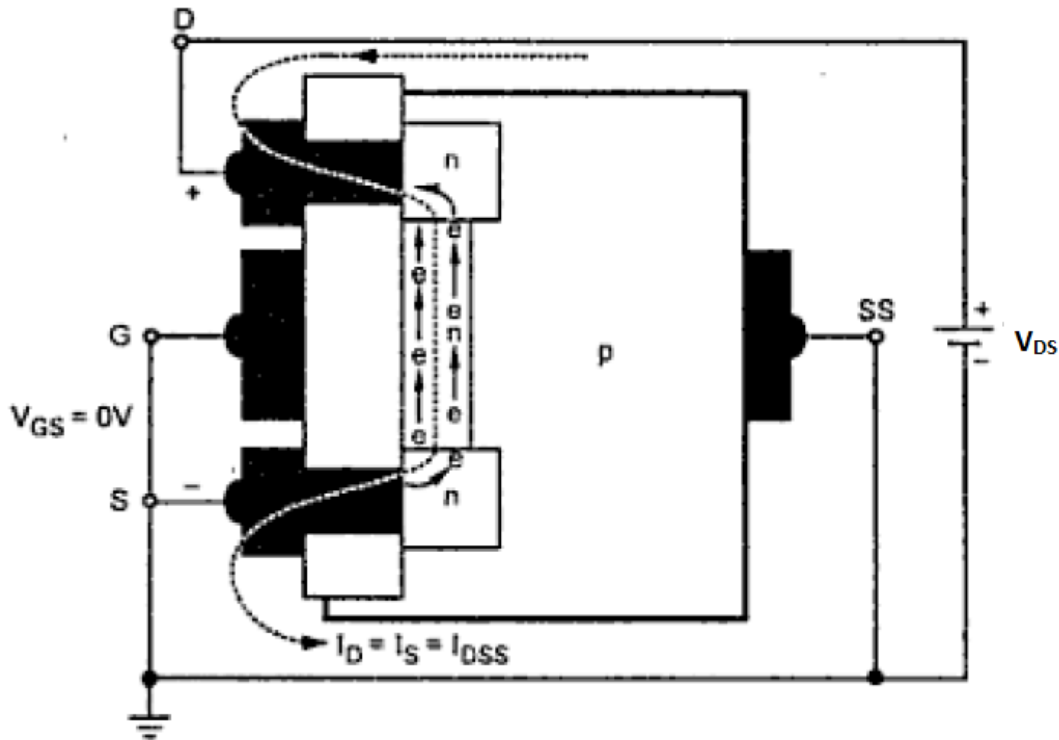


Fig. 2 n-channel depletion-type MOSFET with  $V_{GS} = 0\text{ V}$  and an applied voltage  $V_{DS}$

### Operation with Negative $V_{GS}$ .

Due to negative voltage applied between gate and source terminals, the gate will tend to repel the free electrons towards the p substrate. These electrons and holes will recombine and will reduce the number of electrons available for conduction. Thus, the drain current  $I_D$  will decrease with increase in negative value of  $V_{GS}$ .

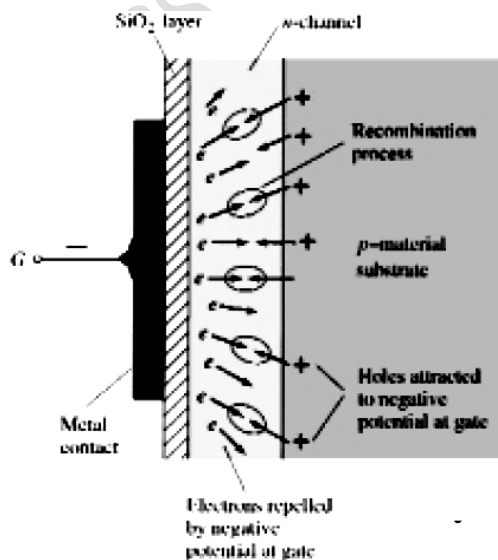


Fig 4 Reduction in free carriers in channel due to a negative potential at the gate terminal.

The higher the negative  $V_{GS}$ , the more is the recombination of electrons and holes & less is drain current.

# MOSFET: Depletion Type

**NOTE-** The level of free electrons are enhance due to the application of positive gate voltage. The region of operation corresponding to the positive gate voltage is called ENHANCEMENT REGION.

## p-Channel Depletion-Type MOSFET

The construction of a p-channel depletion-type MOSFET is exactly the reverse of that N channel Depletion-type MOSFET. That means, there is now an n-type substrate and a p-type channel, as shown in Fig. 5a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as that for N channel Depletion-type MOSFET but with  $V_{DS}$  having negative values,  $I_D$  having positive values as indicated (since the defined direction is now reversed), and  $V_{GS}$  having the opposite polarities as shown in Fig. 5c Shockley's equation is still applicable and requires simply placing the correct sign for both  $V_{GS}$  and  $V_p$  in the equation.

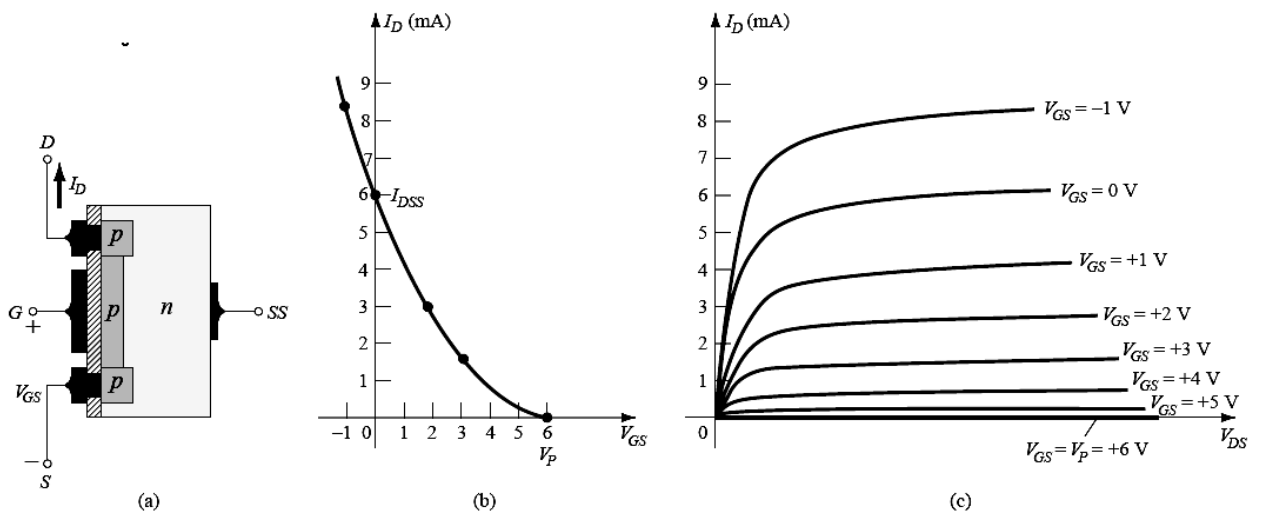
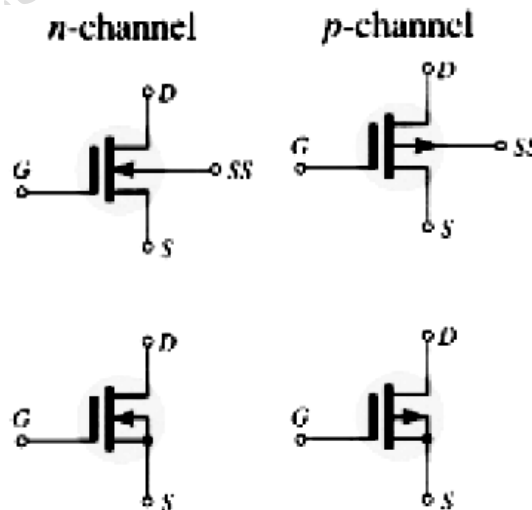


Fig 5 p-Channel depletion-type MOSFET with  $I_{DSS} = 6 \text{ mA}$  and  $V_p = +6 \text{ V}$ .

## SYMBOLS





# MOSFET: Enhancement Type

## ENHANCEMENT-TYPE MOSFET

### Basic Construction (N channel enhancement –type MOSFET)

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig.1. A slab of p-type material is formed from a silicon base and is referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are connected through metallic contacts to n-doped regions, but note in Fig.1 the absence of a channel between the two n-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The  $\text{SiO}_2$  layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

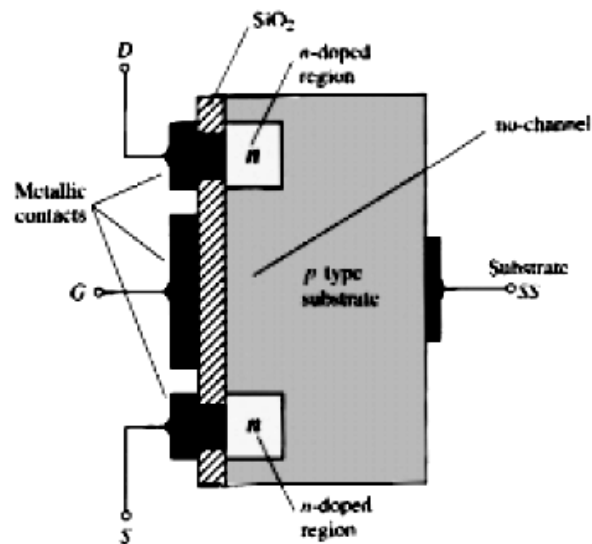


Fig 1

### Basic Operation

#### 1. Operation with $V_{GS}=0V$ and $V_{DS}$ = positive.

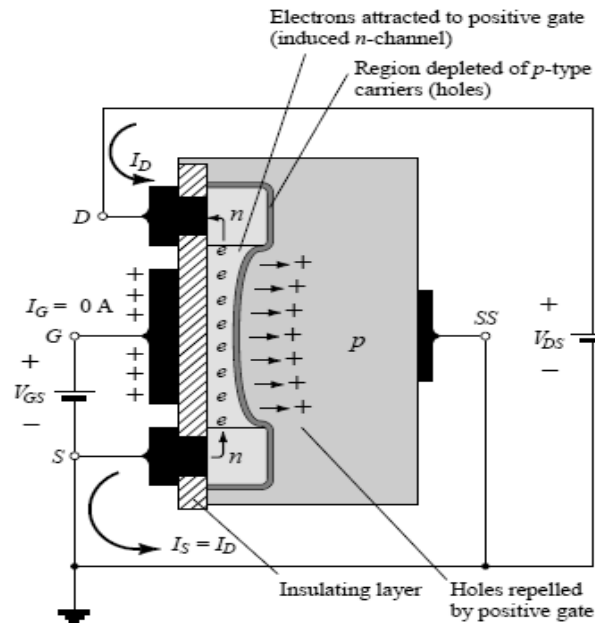
If  $V_{GS}$  is set at 0 V and a voltage applied between the drain and source of the device of Fig.1, the absence of an n-channel (with its generous number of free carriers) will result in a current of 0 Amperes.

#### 2. Operation with $V_{GS}$ = positive and $V_{DS}$ = positive.

In Fig. 2 both  $V_{DS}$  and  $V_{GS}$  have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the  $\text{SiO}_2$  layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure. The result is a depletion region near the  $\text{SiO}_2$  insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the

## MOSFET: Enhancement Type

SiO<sub>2</sub> layer. The SiO<sub>2</sub> layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As  $V_{GS}$  increases in magnitude, the concentration of electrons near the SiO<sub>2</sub> surface increases until eventually the induced n-type region can support a measurable flow between drain and source.



**Fig 2**

**Threshold Voltage ( $V_T$ )** - The level of  $V_{GS}$  at which the channel begins to conduct is called the Threshold Voltage,  $V_T$ . Since the channel is nonexistent with  $V_{GS} = 0$  V and “enhanced” by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET.

As  $V_{GS}$  is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold  $V_{GS}$  constant and increase the level of  $V_{DS}$ , the following conditions results.

1. If  $V_{GS} - V_{DS} > V_T$ , the n channel MOSFET will work in Linear Region, and the drain current  $I_D$  will increase linearly with increase in drain voltage  $V_{DS}$ .
2. If  $V_{GS} - V_{DS} = V_T$ , the gate will become less and less positive with respect to drain. Thus, the number of electrons near to the drain terminal also reduces and channel will be become PINCHED OFF at the drain terminal. (Fig 3)
3. If  $V_{GS} - V_{DS} < V_T$ , the n channel MOSFET will enter into SATURATION. Now, the drain current will not increase, even if we increase  $V_{DS}$  further.

# MOSFET: Enhancement Type

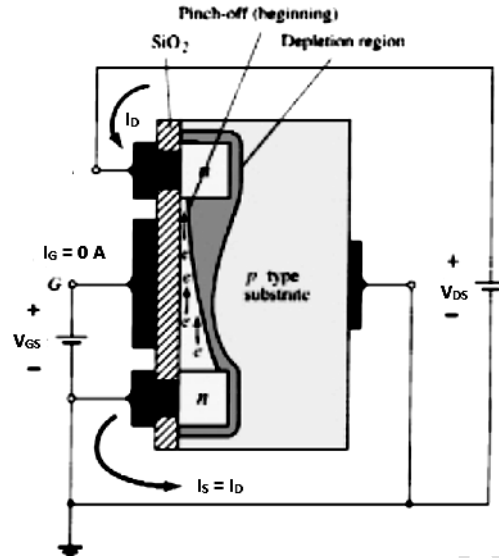


Fig 3

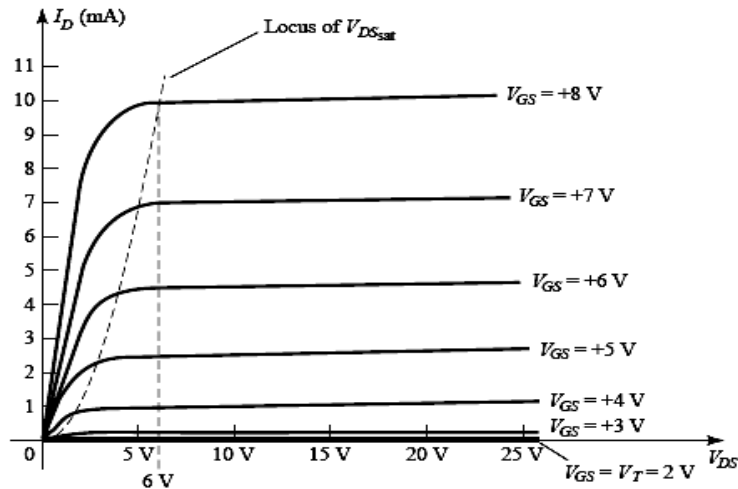


Fig 4 Drain Characteristics

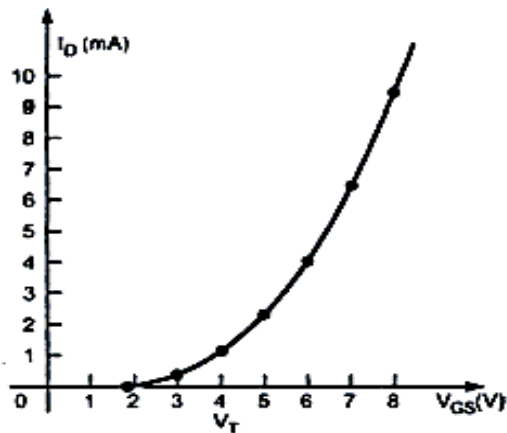


Fig 5 Transfer Characteristics of n channel Enhancement MOSFET

# MOSFET: Enhancement Type

For levels of  $V_{GS} > V_T$ , the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

The  $k$  term is a constant that is a function of the construction of the device.

## P Channel Enhancement type MOSFET

- Structure of  $p$  channel device
  - The substrate is  $n$  type and the inversion layer is  $p$  type.
  - Carrier is hole.
  - Threshold voltage is negative.
  - All the voltages and currents are opposite to the ones of  $n$  channel device.
  - Physical operation is similar to that of  $n$  channel device.

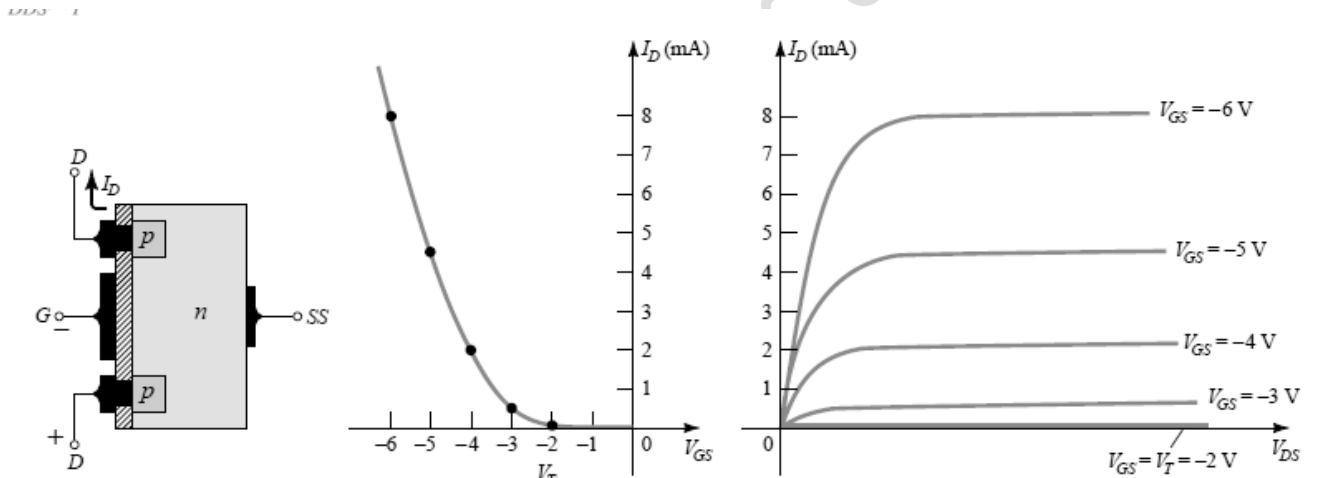


Fig 4 : P channel Enhancement MOSFET construction, Drain Characteristics and Transfer characteristics.

# Transistor Configurations: Common Base

## Transistor Configurations

Depending on which terminal is made common to input and output port, there are 3 possible configurations of the transistor.

1. Common Base Configuration
2. Common Emitter Configuration
3. Common Collector Configuration

## Common Base Configuration

The common-base Configuration, the base is common to both the input and output sides of the configuration. The fig 7 shows p-n-p and n-p-n transistor in Common base mode.

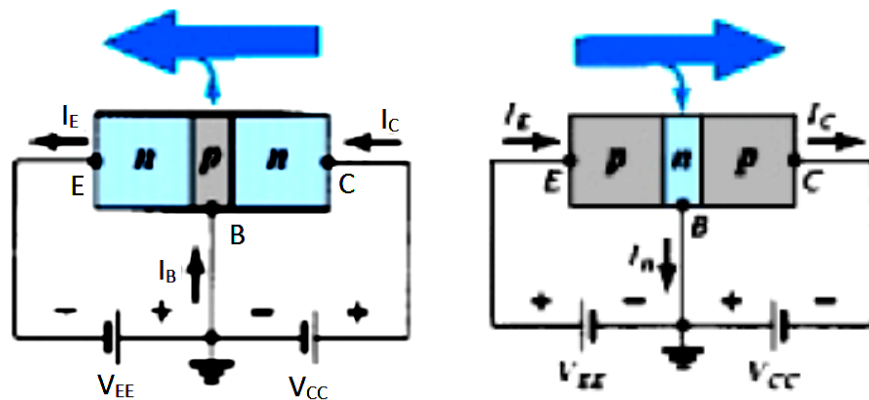


Fig 7

## The Input Characteristics (For n-p-n Common Base Transistor)

The Input Characteristics is graph between input current versus input voltage. The input characteristics relate the input current ( $I_E$ ) to an input voltage ( $V_{BE}$ ) for various levels of output voltage ( $V_{CB}$ ). They are similar to the v-I characteristics of forward biased p-n junction diode.

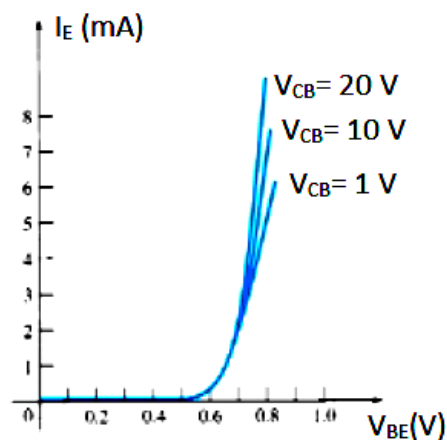
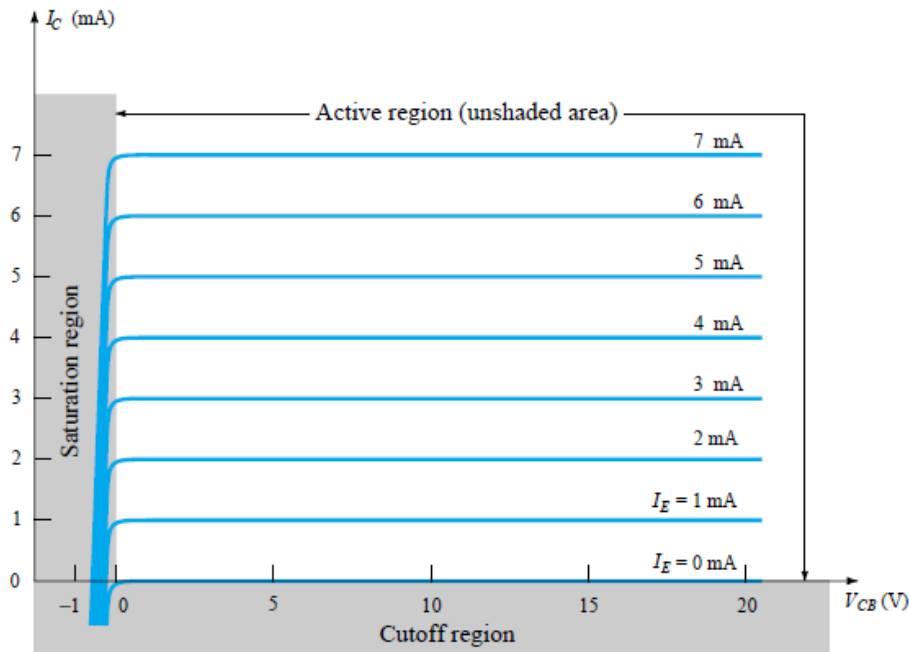


Fig 8: The Input Characteristics for n-p-n common base Transistor

## Transistor Configurations: Common Base

### The Output Characteristics ( For n-p-n Common Base Transistor)

The output characteristics are a graph between output current and output voltage. The output characteristics relate the output current ( $I_C$ ) to an output voltage ( $V_{CB}$ ) for various levels of input current ( $I_E$ ).



**Fig 9: Output Characteristics of n-p-n Transistor**

The figure 9 above, shows three regions

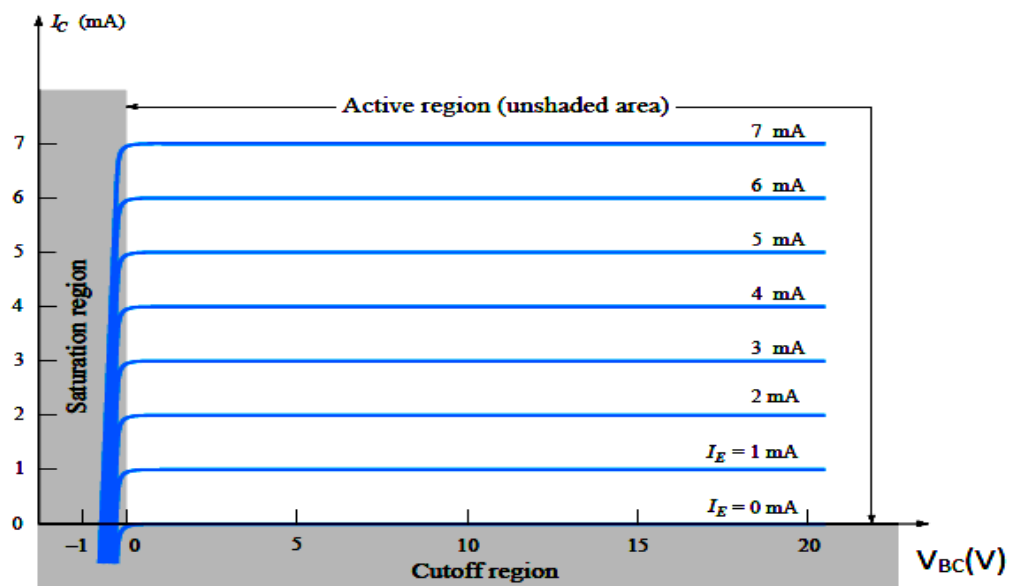
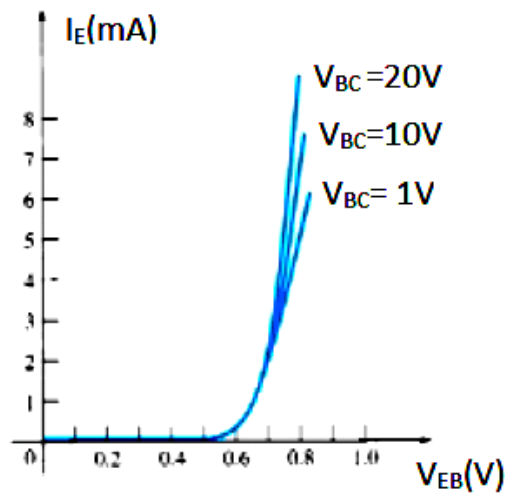
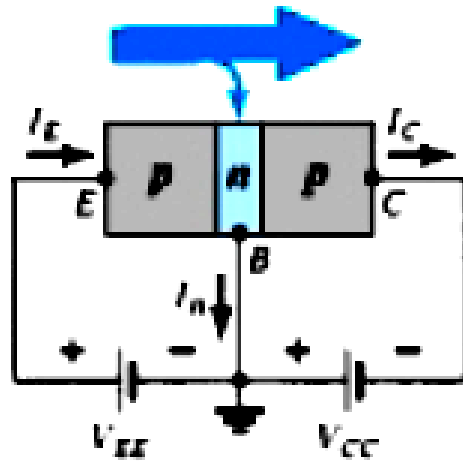
**(a)Active Region-** In active region the Emitter Base junction is forward biased and Collector base junction is Reverse Biased. By biasing the transistor in this region, we can operate it as **Amplifier**.

**(b)Saturation Region-** In Saturation region the Emitter Base junction is forward biased and Collector base junction is Forward Biased. By biasing the transistor in this region, we can operate it as a **Closed Switch**.

**(c)Cutoff Region-** In Cutoff region the Emitter Base junction is Reverse biased and Collector base junction is Reverse Biased. By biasing the transistor in this region, we can be operate it as an **Open Switch**.

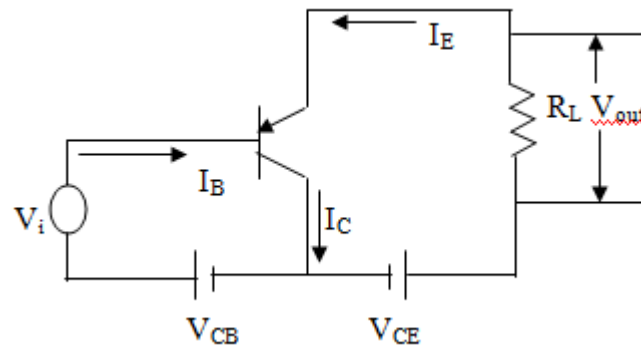
# Transistor Configurations: Common Base

## Input and output characteristics for p-n-p Common Base Transistor



# Transistor Configurations: Common Collector

## CC configuration



**Fig 1: CC configuration**

In this configuration the input is connected between the base and collector while the output is taken between emitter and collector.

Here  $I_B$  is the input current and  $I_E$  is the output current.

## Current relations

1. Current amplification factor ( $\gamma$ )
- 2. Relationship between  $\alpha$ ,  $\beta$  and  $\gamma$**

$$\gamma = \frac{I_E}{I_B}$$

$$\gamma = \frac{I_B + I_C}{I_B}$$

divide both Numerator and denominator by  $I_B$

$$\gamma = \frac{1 + \frac{I_C}{I_B}}{1}$$



## Transistor Configurations: Common Collector

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$$\gamma = 1 + \beta \quad (\beta = I_C / I_B)$$

$$\gamma = 1 + \frac{\alpha}{1 - \alpha}$$

$$\boxed{\gamma = \frac{1}{1 - \alpha}}$$

### Derivation of total output current $I_E$

We know that  $I_C = \alpha I_E + I_{CBO}$

$$I_E = I_B + I_C$$

$$I_E = I_B + \alpha I_E + I_{CBO}$$

$$I_E(1 - \alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha}$$

$$I_E = \gamma I_B + \gamma I_{CBO}$$

$$\boxed{I_E = \gamma (I_B + I_{CBO})}$$

### 3.5 Comparison between CB, CC and CE configuration

Characteristics	CB	CE	CC
1. Input resistance ( $R_i$ )	low	low	high
2. Output resistance ( $R_o$ )	high	high	low
3. Current amplification factor	$\alpha = \frac{\beta}{1 + \beta}$	$\beta = \frac{\alpha}{1 - \alpha}$	$\gamma = \frac{1}{1 - \alpha}$

## Transistor Configurations: Common Collector

4. Total output current	$I_C = \alpha I_E + I_{CBO}$	$I_C = \beta I_B + (1 + \beta) I_{CBO}$	$I_E = \gamma I_B + \gamma I_{CBO}$
5. Phase relationship between input and output	In-phase	Out-of phase	in-phase
6. Applications	For high frequency applications	For audio frequency applications	For impedance matching
7. Current gain	Less than unity	Greater than unity	Very high
8. Voltage gain	Very high	Grater than unity	Less than unity

# Transistor Configurations: Common Emitter

## Common Emitter Configuration

The Emitter is a common terminal between input and output. Here, the input is applied at base and output is taken at the collector.

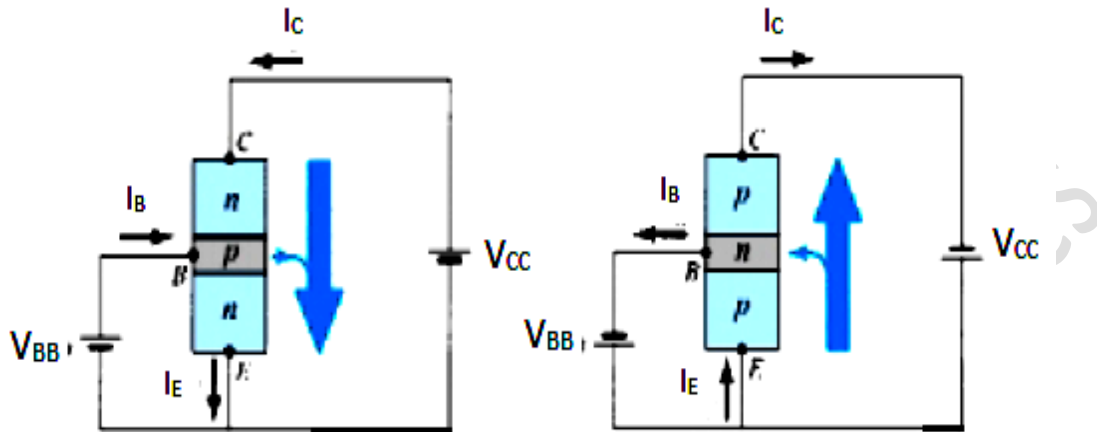


Fig 10

## The Input and Output characteristics (For Common Emitter n-p-n Transistor)

The input characteristics are a plot of the input current ( $I_B$ ) versus the input voltage ( $V_{BE}$ ) for a range of values of output voltage ( $V_{CE}$ ) as shown in fig 11.

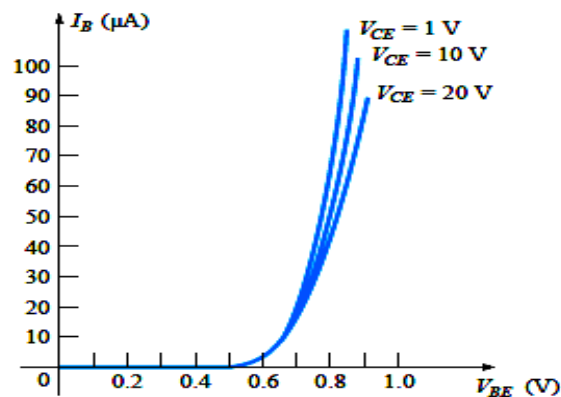


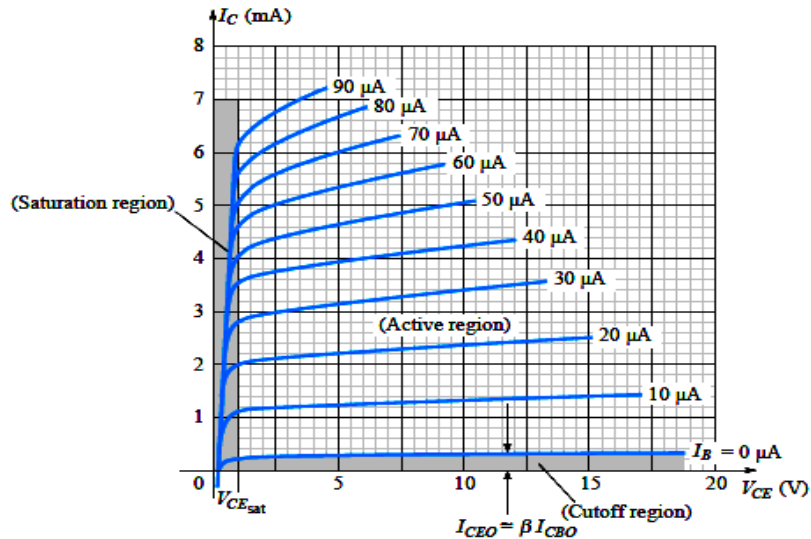
Fig 11

For the common-emitter configuration the output characteristics are a plot of the output current ( $I_C$ ) versus output voltage ( $V_{CE}$ ) for a range of values of input current ( $I_B$ ).

As shown in fig 12, for a fixed value of  $I_B$ , as we increase the  $V_{CE}$ , the collector current increases.

The Region to the right of  $V_{CE(sat)}$  is called saturation region. In this region, both the Emitter Base and Collector Base junctions are Forward Biased.

## Transistor Configurations: Common Emitter



**Fig 12** The output Characteristics of n-p-n Transistor in CE Configuration.

We know,

$$I_E = I_B + I_C$$

**Alpha D.C ( $\alpha_{dc}$ ) =  $I_C/I_E$ , where  $I_C$  is  $I_{C \text{ majority}}$ )**

**Beta D.C ( $\beta_{dc}$ ) =  $I_C/I_B$**

$$I_C = I_{C \text{ majority}} + I_{CO}$$

$$I_C = I_{C \text{ majority}} + I_{CBO}$$

(Since,  $I_{CO}$  is same as  $I_{CBO}$ : collector to base leakage (Minority) current when emitter is open)

**Replace  $I_{C \text{ majority}}$  with  $\alpha I_E$**

We get

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha}$$

If  $I_B = 0$ , then  $I_C$  is

$$I_C = \frac{I_{CBO}}{1 - \alpha}$$

Thus, we call

$$\frac{I_{CBO}}{1 - \alpha}$$

As  $I_{CEO}$  i.e, Collector to Emitter Current with base open circuited.

Hence  $I_C = \{\alpha I_B / (1-\alpha)\} + I_{CEO}$

# Transistor Configurations: Common Emitter

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## The Input and Output characteristics (For Common Emitter p-n-p Transistor)

The input characteristics are same as that for n-p-n transistor, but here  $V_{BE}$  is replaced by  $V_{EB}$  and  $V_{CE}$  is replaced by  $V_{EC}$ .

In output characteristics, the  $V_{CE}$  is replaced by  $V_{EC}$ .

### Relation between $\alpha$ and $\beta$

We know

$$I_E = I_C + I_B$$

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

### Relation between $I_{CBO}$ and $I_{CEO}$

We know

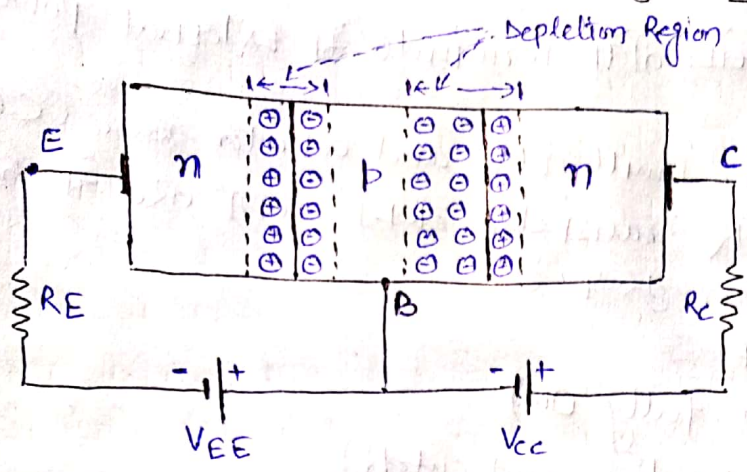
$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

$$\frac{1}{1 - \alpha} = \beta + 1$$

$$I_{CEO} = (\beta + 1)I_{CBO}$$

$$I_{CEO} \cong \beta I_{CBO}$$

# Transistor operation in Active Region (n-p-n)



BE junction is Reverse Biased  
 CB junction is forward biased  
 RE and RC are current limiting resistors.

- \* Due to forward bias of BE junction Polas होने के कारण BE junction पर depletion region कम हो जाता है।
- \* CB junction पर Reverse Bias होने के कारण CB junction पर depletion region ज्यादा होता है जो कि Base Region में ज्यादा होता है।

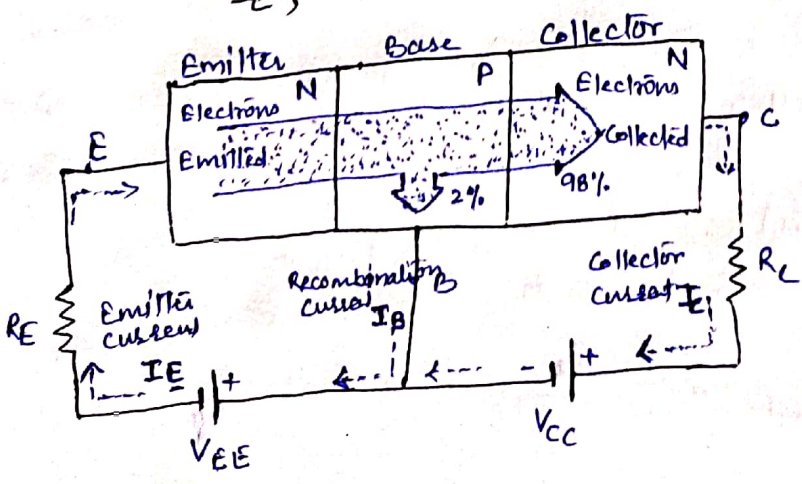
## operation :-

\* n-type emitter के electrons जो कि majority carriers हैं, p-type base की तरफ flow करते हैं जिसकी वजह से

Emitter current  $I_E$  flow करना start करती है।

- \* Emitter से Base में आने वाले electrons के पास तीन options होते हैं
  1. वे Base के holes के साथ recombine कर सकते हैं, परंतु Base region पतला और कम doping का होने के कारण वहाँ बहुत कम संख्या में holes होते हैं। अतः Emitter से आये हुए बहुत कम electrons, बेस के holes से recombine करते हैं, electrons (Emitter) के holes (Base) से recombine करने के कारण बहुत थोड़ी सी बेस current ( $I_B$ ) बहती है।  
 $I_B, I_E$  का लगभग 2% होती है।
  2. कुछ electrons base connection से diffusion के द्वारा बाहर निकल जाते हैं।
  3. बचे हुए ज्यादातर (98%) electrons, CB junction के depletion region को पार करके collector region के पार  $V_{CC}$  के positive terminal तक पहुँच जाते हैं, जिस कारण collector current ( $I_C$ ) flow करती है।  
 $I_C, I_B$  से बहुत ज्यादा होती है।

$$I_E = I_C + I_B$$

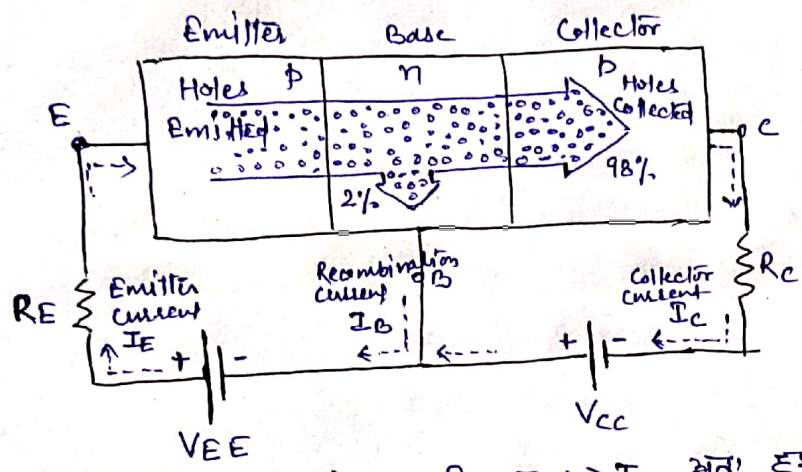


Note :- चित्र में current की direction flow of electrons की दिशा में दर्शायी गई है, जबकि conventional current की direction, flow of positive charge की दिशा में होती है। अतः वास्तविक current flow की direction विपरीत दिशा में होगी।

### Operation of p-n-p Transistor in the Active Region

- \* p-n-p Transistor विकृत n-p-n Transistor की तरह Behave करता है।
- \* केवल अंतर यह है कि यहाँ majority charge carriers holes होते हैं।
- \* Emitter से holes emit होते हैं। क्योंकि Emitter p-type होता है। Emitter से निकले होल EB junction (जोकि forward biased है) को cross कर n-type Base में पहुँचते हैं।
- \* कम doping वाले Base में बहुत कम संख्या में electrons होते हैं जो Emitter से आये हुए holes से recombine करते हैं जिस वजह से कम मात्रा में बेस current ( $I_B$ ) बहती है।
- \* अतः 2% of Total बेस बेस के electrons से recombine करते हैं और 98% holes collector से होते हुए  $V_{CC}$  के -ve terminal तक पहुँचते हैं जिस कारण से collector current ( $I_C$ ) बहती है।

$$I_E = I_C + I_B$$

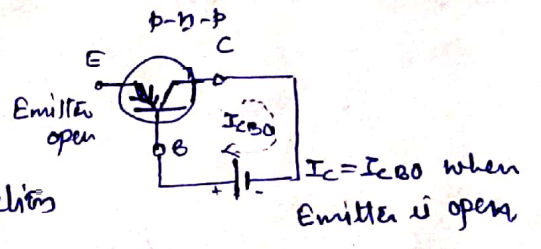


\* चित्र में current की direction flow of holes (+ve charge) की direction में दर्शायी गई है जोकि conventional current (वास्तविक current) की direction है।

जैसा कि हमने देखा कि  $I_C \gg I_B$  अतः हम कभी-कभी ये भी मानकर चलते हैं कि  $I_E \approx I_C$

### Reverse Saturation Current ( $I_{CBO}$ ) in a transistor :

- \*  $I_{CBO}$  (Reverse Saturation Current) वे current है जो collection junction से बहती है जब Emitter junction open होता है।
- \*  $I_{CBO}$  minority carriers की वजह से बहती है अतः Temperature बढ़ने पर  $I_{CBO}$  का मान बढ़ता जाता है।  $I_{CBO}$  को collector to Base leakage current भी कहते हैं।
- \* p-n-p के case में minority carriers, n-type base के electrons होते हैं जो n-type base से p-type collector की तरफ जाते हैं।
- \* Collector Current (Total)



$$I_C = I_C(\text{holes}) + I_{CBO}(\text{electrons})$$

$$I_C = I_C(\text{majority}) + I_{CBO}$$